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JC529 U.S. PTO 02/27/98

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P4750	*Total Pages*	36
First Named Inventor or Application Identifier			
Lawrence T. Clark			
Express Mail Label No.	EM560821934US		

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 22] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 CFR 113)* [Total Sheets 6]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(usable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: . . . . . .

17. **If a CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number of Bar Code Label* *(Insert Customer No. or Attach bare code label here)* or [X] *Correspondence address below*

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FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 830.00

Complete if Known	
Application Number	
Filing Date	2/27/98
First Named Inventor	Lawrence T. Clark
Group Art Unit	
Examiner Name	
Attorney Docket Number	042390.P4750

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 ☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.311(b)

2. ☒ Payment Enclosed:
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FEE CALCULATION (fees effective 10/01/96)

1. FILING FEE

Large Fee Code	Large Fee ($)	Small Fee Code	Small Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. CLAIMS

		Extra		Fee from below		Fee Paid
Total Claims	16	-20 =	0	X 22.00	=	$0.00
Independent Claims	3	-3 =	0	X 82.00	=	$0.00
Multiple Dependent Claims					=	

Large Fee Code	Large Fee ($)	Small Fee Code	Small Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple Dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Fee Code	Large Fee ($)	Small Fee Code	Small Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (2) ($) 40.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Eric S. Hyman, Reg. No. 30,139			Reg. Number	
Signature		Date	2/27/98	Deposit Account User ID	02-2666

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Docket No. 042390.P4750
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UNITED STATES PATENT APPLICATION FOR

Photodetecting Device Supporting Saturation Detection and Electronic Shutter

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BACKGROUND INFORMATION

This invention is generally related to analog signal processing and more particularly to imaging sensors.

Electronic sensors that respond to incident electromagnetic radiation such as light are used in a wide range of applications, from the simple infrared photodetector used in home security systems to complex medical imaging applications. Such sensors provide electrical signals in relation to the energy incident on the sensor. One particular type of sensor is the imaging sensor used for capturing images of objects or scenes from which light energy has been reflected. Such sensors are found in consumer products such as video cameras, scanners, copiers, and, more recently, digital cameras which provide images in a computer-readable format.

A typical imaging sensor is a circuit composed of a number of active semiconductor photocells usually arranged as an array. Examples include the complimentary metal oxide semiconductor (CMOS) active pixel sensor (APS). Each photocell of an imaging sensor has a photodetector and associated control and readout circuitry (including active devices such as transistors). Photogenerated charge in the cell causes a signal to be generated that is a measure of the energy that was incident on the cell. The cell may also feature a saturation limiting circuit which can be used to limit the response of the photocell to the incident energy, and/or an electronic shutter facility which can capture a signal representing the detected incident energy at a specific time.

After the array has been exposed to the object or scene and incident energy has been detected, the signals from the individual cells of the array are collected

and may be converted to digital format. This digital image data represents the image that was formed on the sensor array. The digital image data can then be manipulated and displayed using known signal and image processing techniques to yield a desired image size and quality.

One of the problems encountered with imaging sensors is saturation. Saturation occurs when one or more cells in the sensor have been exposed to too much incident energy in view of its dynamic range, i.e., ability to respond faithfully to changes in incident energy. When saturated, the cell output changes too little or not at all in response to more incident energy. An example of the effect of saturation is seen in images as very bright or almost white regions which correspond to saturated cells in the sensor array.

Saturation can be avoided by controlling an electronic shutter circuit in each photocell to limit the total energy detected by the photocell. Some cells provide a signal that represents the instantaneous detected energy and is controlled by the electronic shutter. The signal is integrated over a time interval known as the exposure or integration interval to obtain the total energy. Saturation is avoided in such cells by reducing the integration interval and by controlling the electronic to prevent the signal from reaching a saturation level.

To help determine the proper interval in such imaging systems, a light level test of the scene may be conducted prior to obtaining an image of the scene. During the light level test, the sensor array is exposed to the scene to identify those cells which are receiving strong light and are therefore saturated. Thereafter, the integration intervals for those cells are reduced, and the array is again exposed to the same scene but with the reduced integration times. Lowering the integration interval lowers the amount of incident energy that is

detected by the photocell. In a perfect imaging system, the integration times are adjusted so that the cells are allowed to detect the incident energy up to the dynamic range without saturating any cells.

However, the above technique requires the user or the imaging system to guess at the optimum integration interval that avoids saturation yet maximizes dynamic range for the affected photocells. If the integration interval is reduced too much, then dynamic range is reduced as the photocell may still be able to accurately detect more incident energy; if the integration interval is not reduced enough, the photocells can still saturate. Also, taking multiple exposures of the same scene as required by the above technique may prove to be too slow for rapid frame rate applications such as movies.

Therefore, a better technique of preventing saturation in photocells and sensor arrays is desirable that helps maximize dynamic range. Such a technique should also be capable of integration with the manufacture of other electronic circuits, such as those built using standard metal oxide semiconductor (MOS) fabrication processes that are typically used to implement digital functions. In addition, the novel photocell design should be compact to allow improved manufacturing yields in large and dense sensor arrays.

SUMMARY

In one embodiment, this invention is directed at a photodetecting device having a first region of semiconductor material of a first conductivity type, and a second region of semiconductor material of a second conductivity type opposite the first conductivity type and extending over a portion of the first region. The device is configured to permit light to enter the second region. In addition, third and fourth regions of semiconductor material of the first conductivity type are provided extending over portions of the second region, where the third and fourth regions are respectively coupled to electrical contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features as well as advantages of the different embodiments of the invention will be apparent by referring to the drawings, detailed description and claims below, where:

Figure 1 illustrates a photocell according to an embodiment of the invention.

Figure 2 is a top view of a portion of the photocell implemented using an n-well semiconductor fabrication process according to yet another embodiment of the invention.

Figure 3 is a cross section view of the semiconductor structure of **Figure 2**.

Figure 4 is a flow diagram of steps performed according to another embodiment of the invention.

Figure 5 illustrates various waveforms associated with operation of a photocell similar to the one in **Figure 1**.

Figure 6 illustrates a sensor array according to another embodiment of the invention.

Figure 7 shows a logical block diagram of an imaging system according to another embodiment of the invention.

DETAILED DESCRIPTION

As briefly summarized above, an embodiment of the invention is directed at a photocell that can help peripheral circuitry detect a near saturation condition of the photocell while the cell is measuring incident energy. The peripheral circuitry can be configured to stop integration and therefore avoid saturation of the photocell while at the same time take advantage of the cell's full dynamic range. The photocell has a photodetecting device with two electrical contacts, one of which is used for saturation detection and the other is coupled to a sample node that supports an electronic shutter mechanism. When implemented using a standard MOS fabrication process, the detecting device is a multi-emitter parasitic bipolar junction transistor (BJT). In that embodiment, the photocell also makes efficient use of transistors with only four MOS devices, including an optional one for the storage capacitance associated with the electronic shutter mechanism, in addition to the photodetecting device being the parasitic BJT.

The novel cell can be used as part of a sensor IC in a variety of imaging applications to improve the final image quality by avoiding saturation yet taking advantage of the full dynamic range of a cell, and improve manufacturability by keeping the sensor IC compact using relatively inexpensive CMOS fabrication techniques.

The sensor cells in an array (as part of sensor IC) may be monitored for saturation on a per column or row basis. The integration intervals may also be controlled on a per column or per row basis. If the sensor array is exposed to a scene having strongly lit areas, the photocells in a column or row detecting those areas will tend to saturate before the rest of the scene has been adequately

detected. The embodiments of the invention allow the row or column receiving strong light to be identified, its saturation to be prevented by ending integration for the affected row or column, and simultaneously continuing to integrate other rows or columns that received low light. This allows a more accurate image of the scene, closer to one obtainable from a perfect imaging system, to be captured in which both low and strong light areas are represented free of saturation effects and using a single exposure.

Operation of the various embodiments of the invention will be explained using a MOS implementation of the circuits. The following short cuts are used in this disclosure to describe various operating regions of the MOS field effect transistor (FET). A FET is said to be "turned off" when V_{GS} (gate-source voltage) $< V_T$ (threshold voltage for the device and the device is operating in the cut-off region where its channel, to a first order, acts as an open circuit. When a FET is "turned on", $V_{GS}>V_T$, V_{DS} (drain-source voltage) is normally small and the device is operating in the non-saturation region. In certain cases, the FET is also deemed to be turned on when conducting in its linear or saturation regions.

Figure 1 illustrates the first embodiment of the invention as a sensor 100. The figure illustrates the photocell in terms of a circuit schematic featuring a BJT Q_1 that operates as a photodetector. In a particular embodiment, the photocell 100 is implemented using a standard logic complimentary MOS (CMOS) fabrication process in which Q_1 is a PNP parasitic device built using a single n-well with highly doped p+ regions (such as implants) that may correspond to an unrealized MOSFET extending over portions of the n-well 204. Thus, Q_1 is realizable with a conventional CMOS process rather than a more expensive Bipolar-CMOS (Bi-CMOS). The p+ regions 208 and 212 are connected to electrical

contacts that form the global emitter (GE) and pixel emitter (PE) contacts shown in **Figure 1**. A top view of Q_1 in this embodiment is illustrated in **Figure 2**, while **Figure 3** shows Q_1, being a parasitic PNP device, by way of cross section. It can be seen that the p-region 304 forms part of the collector of Q_1, the n-well 204 forming part of the base, and the p+ regions 208 and 212 forming the multiple emitters.

The device Q_1 in one embodiment operates as a photodetector by having a translucent opening above the n-well (the field oxide 308 is translucent) as shown for incident light to pass through and enter the n-well. Portions of the n-well 204 and the well 204-to-substrate 304 junction of Q_1 form the photosensitive portion of the device. The response of Q1 to incident light may be tailored using various MOSFET source/drain implants for the 208 and 212 regions. This may be useful as a CMOS salicided process may be used, where the silicide (not shown) that covers the 208, 212 and optionally 216 regions is opaque (to a first order) to light. In addition to using different implants, a silicide blocking mask may be used to increase the opening for incident light.

As part of the photocell 100, the device Q_1 is a multiple emitter parasitic transistor, where a first emitter PE is coupled to a storage device M_6 and a transistor M_5 at a "SAMPLE" node. Sensitivity to incident light is enhanced over a MOS-only implementation of the cell, because the gain β of the parasitic BJT is greater than one. M_6 provides capacitance large enough to hold the charge to that which is needed to obtain a desired dynamic range for the photocell given the leakage currents through SAMPLE and given the speed with which circuitry external to the photocell 100 can read the output voltage at node "BL". However, M_6 may be eliminated if the leakage at SAMPLE is small enough and the node

otherwise exhibits enough parasitic capacitance to hold a signal level until the output voltage is read. The output may be read after asserting Cell_Readout.

M_5 operates as a reset transistor to pull SAMPLE up to a value at or near the rail voltage, a so-called reset value. M_5 receives a signal Reset_E which, in one embodiment, is designed to overdrive the gate of M_5 with a signal that is sufficiently above V_{DD} so that SAMPLE is pulled up to a value that is as close as possible to the rail voltage V_{DD}. This helps overcome the body-effect of the n-channel transistor M5 which otherwise may prevent SAMPLE from reaching V_{DD}. Pulling sample up to V_{DD} increases the dynamic range of the photocell by providing a higher reset value at SAMPLE at the start of the integration interval.

Also connected to SAMPLE is a readout circuit RCKT that provides the photocell's output signal. The function of RCKT and the load device at BL is to drive BL when the cell has been selected in response to a signal Cell-Readout. RCKT in the embodiment of **Figure 1** includes a transistor M_2 operating as a source follower and an output select pass gate RCKT transistor M_1. In response to the external signal Cell_Readout, RCKT provides an output signal across the load device at BL. To reduce the physical size of the photocell, RCKT is kept simple and the load device is outside the photocell. However, other readout circuit configurations and loads are possible and may be developed by those skilled in the art.

Returning now to the device Q_1, its second emitter contact GE is connected to a "MONITOR" node which in turn is connected to a stop circuit SCKT and a number of GE contacts in other identical cells, shown collectively as cells $100A_1$, $100A_2$, ... in **Figure 6**. As explained below, the voltage at MONITOR will follow

the lowest GE voltage from all other connected cells, and represents the cell which is approaching saturation the quickest.

The stop circuit SCKT in this embodiment includes a single transistor MP_1 that provides a load to the emitter GE of Q_1 and receives a Reset_GE signal which turns it on and off. The Reset_GE signal when asserted turns MP_1 on thereby pulling MONITOR up to a voltage close to the rail. Other configurations are possible for SCKT which provide a suitable load to GE as well as pull MONITOR to a voltage sufficiently high to cut off collector current through Q_1.

A control circuit CCKT is coupled between MONITOR and SCKT. In one embodiment, CCKT asserts Reset_GE when MONITOR has reached a predetermined level. This indicates that one of the cells connected to MONITOR is approaching saturation. Asserting Reset_GE in turn pulls the base of each Q_1 in the connected cells up to a voltage at or near the rail, thereby reverse biasing the PE junctions in each Q_1. This, as explained further below, causes the last value at SAMPLE in each cell to be captured in each cell.

In the embodiment of **Figure 1**, Q_1 is shown as having a base that is floating. However, an n+ region 216 may optionally be added over the n-well 204 together with a base contact, as shown in **Figures 2 and 3,** if needed for biasing Q_1. Biasing circuits known to those skilled in the art may be attached to the base contact.

The operation of photocell 100 may be illustrated using the steps of **Figure 4** and the waveforms in **Figure 5**. Operation begins in step 414 with SAMPLE being precharged to a reset value, such as one near the rail voltage V_{DD} (e.g., 3.3 volts) by way of turning on transistor M_5. In one embodiment, M_5 can

receive an overdriven gate voltage through signal Reset_E to mitigate body-effect in M_5 and drive SAMPLE to a voltage very close to V_{DD}. This occurs between times 0 and 2 in **Figure 5**. Similarly, MONITOR is also raised to a high level by either turning on MP_1 in response to Reset_GE being deasserted, or by way of a separate and optional pull-up circuit and control signal (not shown). The above operations thus place the photocell 100 in its reset state. Note that step 410 of exposing the photocell to incident energy such as light may be started before or after placing the photocell in its reset state, thus not requiring a separate mechanical shutter when using the cell as part of an imaging sensor.

By time 3, the signals Reset_GE and Reset_E have been de-asserted, as in step 418, thus releasing SAMPLE and beginning the integration interval. During the integration interval, the photocell is allowed translate the incident energy into an electrical signal at SAMPLE. The incident energy causes a photogenerated base current in Q_1 that results in lowering the base voltage of Q_1 towards zero (ground). Q_1 acts as an emitter follower in that both emitters GE and PE follow the base voltage, with the differential of V_{BE} (base to emitter voltage). As the base voltage drops towards 0, both emitters GE and PE may join each other as shown in **Figure 5** and follow the base.

The control circuit CCKT monitors the voltage at MONITOR to detect when the photocell 100 is approaching saturation, as indicated in step 422. Saturation for the photocell 100 of Figure 1 occurs when the SAMPLE voltage has dropped so low that the readout circuit RCKT can no longer follow in a faithful manner. For example, this can occur when the voltage at SAMPLE is insufficient to turn on M_1. Once this threshold level has been determined (either empirically or through design), CCKT may be designed to detect a voltage near

such a level on MONITOR. As MONITOR is connected to the GE contact of a number of other identical cells in a group (e.g., part of a sensor array), the voltage on MONITOR will represent the cell closest to saturation.

When the MONITOR voltage reaches a predetermined level that indicates a near saturation condition, the Reset_GE signal is asserted, signifying the end of the integration interval in step 426. In the timing diagram of **Figure 5**, this occurs at approximately time 9. When Reset_GE is asserted, MONITOR is driven to a stop value (e.g. near V_{DD})which in turn drives the base of Q_1 to V_{DD}-V_{BE} by forward biasing the GE-base junction of Q_1. This in turn reverse biases the PE-base junction, because the stop value is normally selected to be greater than the voltage at SAMPLE at the end of integration, thereby isolating SAMPLE (assuming that M_5 remains off).

Some capacitive coupling between the base and PE is observed as the SAMPLE voltage in **Figure 5** exhibits a slight jump in value at the point integration is terminated. Thus, at low levels of incident energy where the SAMPLE voltage has been driven only slightly lower than its reset value, the SAMPLE node is weakly isolated. However, the effects of this coupling may be canceled by subsequent hardware or software signal processing. In addition, increasing the capacitance of SAMPLE (e.g., larger M_6) may improve isolation of SAMPLE but at the expense of lower sensitivity.

In step 428, the time at which MONITOR is pulled high, and/or the integration time interval (here being 9-3=6 time units) for the group of cells connected to MONITOR is stored by the imaging system. This interval is then used to compute the energy that was incident on the group of cells after obtaining the photocell output values at BL in step 430.

After SAMPLE is isolated in step 426, the output value of the photocell may be read in step 430. This is done by reading the voltage at BL between times 9 and 11 after asserting a Cell_Readout signal. Note that the output voltage at BL will not show any saturation effects, because Reset_GE was timely asserted before the voltages at SAMPLE and MONITOR had reached their saturation level.

The photocell 100 and other variations described above may be used as part of a sensor array 600 having thousands of such cells, as illustrated in **Figure 6**. The sensor array has a number of photocells $100a_1$, $100a_2$ ... $100b_1$, $100b_2$, ... arranged in rows and columns. In the embodiment shown, each column of photocells is connected to a respective monitor node $MONITOR_i$ that is controlled by a respective stop circuit $SCKT_i$ and control circuit $CCKT_i$ that may be similar to the ones described above in connection with **Figure 1**. A global Reset_E signal is applied to all photocells of the array. Each column of photocells also shares a bitline, where an optical image incident on the array is represented by the photocell output signals (sensor signals) obtained through the bitlines.

The architecture of **Figure 6** permits monitoring the sensor array on a per column basis for photocells that are nearing saturation. This may be done by sensing the monitor nodes to detect a near saturation voltage level. Because of the parasitic BJT structure of Q_1 in each photocell of a column, the voltage on a monitor node will follow the lowest Q_1 base voltage in the respective column.

Once a column having a photocell that is near saturation is detected, the imaging system may terminate the integration interval for that column by asserting the Reset_GE signal for that particular column. This integration interval is then stored and used to compute the incident energy for that column. Once integration has ended for the entire sensor array 600, the sensor signals can

be read through the bitlines one row at a time by asserting the appropriate wordline signal on a per row basis, where the wordline signal corresponds to the Cell_Readout signal received by the photocell of **Figure 1**. The detected energy levels are then computed for the entire sensor using the integration intervals for each column, resulting in image data that is closer to the perfect image that can be obtained using the sensor.

Although **Figure 6** shows the monitor nodes being common to columns of photocells, there are alternatives which may be useful depending on the system design. One alternative is to connect the monitor nodes to rows of photocells. In that embodiment, integration is stopped on a per row basis in response to detecting a near saturation condition in a row, and the sensor signals are read one column at a time. In another embodiment, a single monitor node may be used for the entire sensor array, to detect the first photocell that is nearing saturation. Integration may then be terminated simultaneously for all photocells in the array by pulling up the monitor node.

Peripheral circuitry including the timing logic for the various control signals received by the photocells in the sensor array are not shown but they can be readily implemented by one skilled in the art. The sensor array 600 and its peripheral circuitry may be implemented using a standard CMOS logic fabrication process to implement, for instance, a single chip CMOS active pixel sensor. The stop and control circuits $SCKT_i$ and $CCKT_i$ may also be integrated on the same chip together with the sensor array 600.

The sensor array 600 and its alternatives described above may be used as part of a digital imaging system 700 shown in logical block diagram form in **Figure 7**. The imaging system 700 has an optical system 730 that channels the

incident energy being visible light in one case to create an optical image on the sensor array 600. Control signal generation circuitry 718 is provided to detect the signals on the monitor lines and generate the reset signals and wordlines needed to control the photocells of the sensor array 600. The output values (sensor signals) may be further processed in analog form before being fed to an A/D conversion unit 610 which in turn feeds digital processing block 614. Analog signal processing including stop and control circuits $SCKT_i$ and $CCKT_i$, the A/D unit, and portions of the digital processing block may be located on the same die as the sensor array 600. The digital processing may be done by hardwired logic and/or a programmed processor that performs a variety of digital functions, including preparing digital image data based on the sensor signals for storage or transmission.

Transmission of the image data to an external processing system may be accomplished using the communication interface 724. For instance, as a digital camera, the system 700 will contain a communication interface that implements a computer peripheral bus standard such as universal serial bus (USB) or IEEE 1394-1995. The imaging system 700 may also contain a local storage 728 of the non-volatile variety, for instance including a solid state memory such as a removable memory card, a rotating magnetic disk device, or other suitable memory device for permanent storage of digital image data. The operation of the system 700 may be orchestrated by a system controller 722 which may include a conventional microcontroller responding to instructions stored as firmware. The system controller may be programmed to respond to a detected near-saturation condition by storing the integration time values mentioned above in memory, and associating these values with the corresponding group of cells that has reached a near-saturation condition.

To summarize, the above embodiments of the invention feature a photocell 100 having a photodetecting device being a parasitic BJT that may be formed using a standard CMOS process. The parasitic device has a multi-emitter structure that allow monitoring the photocell for saturation in addition to supporting an electronic shutter mechanism, to avoid saturation while at the same time allows the full dynamic range of the photocell to be utilized. The photocell design is particularly compact which helps promote its use as part of a large sensor array.

The embodiments described above are, of course, subject to other variations in structure and implementation. For instance, the photocell 100 may be designed and built with p-channel MOSFET devices instead of the n-channel ones shown in **Figure 1**. M5 may be replaced with a p-channel device formed in a p-well (assuming an n-substrate), but this may increase the size of the cell. In another variation, the photocell may be designed to operate with a dual emitter NPN structure for Q_1 rather than the PNP version described. Therefore, the scope of the invention should be determined not by the embodiments illustrated but by the appended claims and their legal equivalents.

CLAIMS:

What is claimed is:

1. A photodetecting device comprising:

a first region of semiconductor material of a first conductivity type;

a second region of semiconductor material of a second conductivity type opposite the first conductivity type and extending over a portion of the first region, the device being configured to permit light to enter the second region;

third and fourth regions of semiconductor material of the first conductivity type extending over portions of the second region, the third and fourth regions being respectively coupled to first and second electrical contacts.

2. The device of claim 1 wherein the first conductivity type is P and the second conductivity type is N.

3. The device of claim 1 wherein the third and fourth regions are more heavily doped than the first region.

4. A method of using a photocell, comprising

exposing the photocell to incident light;

driving a sample node of the photocell to a reset value;

sensing a monitor node of the photocell, the signal values of the monitor and sample nodes decaying in response to the incident light; and

driving the monitor node to a stop value in response to the signal value of the monitor node having decayed to a predetermined value.

5. The method of claim 4 further comprising:

releasing the sample node after driving the sample node to the reset value;

storing a first time value corresponding to the point in time of releasing the sample node; and

storing a second time value corresponding to the point in time of driving the monitor node.

6. The method of claim 4 wherein exposing is started after driving the sample node.

7. The method of claim 4 further comprising:

reading an output value related to the signal value of the sample node.

8. An imaging system comprising:

an image sensor having a plurality of photocells, the photocells providing sensor signals in response to incident light and control signals, the photocells being part of an integrated circuit (IC) die, the IC die having a first region of semiconductor material of a first conductivity type, each of the plurality of photocells having

a second region of semiconductor material of a second conductivity type opposite the first conductivity type and extending over a portion of the first region, the IC die being configured to permit the incident light to enter the second region,

third and fourth regions of semiconductor material of the first conductivity type extending over portions of the second region, the third and fourth regions respectively coupled to first and second electrical contacts;

control circuitry configured to generate the control signals for controlling the image sensor; and

signal processing circuitry for generating image data in response to the sensor signals.

9. The imaging system of claim 8 wherein the plurality of photocells define one or more sets of photocells, each set being associated with a respective monitor node, the second contact of each photocell in a set being coupled to the set's respective monitor node, the system being further configured to stop integration in one or more of the sets in response to detecting a predetermined value on the set's respective monitor node.

10. The imaging system of claim 8 wherein the plurality of photocells define one set associated with a single monitor node.

11. The imaging system of claim 8 wherein the plurality of photocells are arranged as an array and define a plurality of sets, each set defined by a column of the array.

12. The imaging system of claim 8 further comprising

system controller for controlling the signal processing circuitry.

13. The imaging system of claim 8 further comprising

optical system configured to receive the incident light to form an image on the image sensor; and

communication interface for transferring the image data to an image processing system separate from the imaging system.

14. The imaging system of claim 8 wherein the third and fourth regions are formed as implants using a MOS fabrication process.

15. The imaging system of claim 8 wherein each photocell further comprises reset circuit configured to drive a voltage of the first contact to a reset value in response to a first reset signal.

16. The imaging system of claim 9 wherein the control circuitry causes the set's respective monitor node to be pulled high in response to detecting the predetermined value.

ABSTRACT

Imaging system having a sensor array with photocells that permit the monitoring of light levels while the sensor is exposed to a scene, and the ability to accurately avoid saturation on a per column, row, or array basis. The sensor array supports variable dynamic range by allowing variable integration times for different columns or rows of the array, thereby improving image quality of a scene in which there are both strong and weak light areas. In one embodiment, the photocell includes a parasitic multi-emitter bipolar junction transistor (BJT) acting as a photodetector. The parasitic device is part of a saturation detection circuit and also supports an electronic shutter mechanism. The parasitic BJT also permits increased sensitivity over some previous CMOS approaches. The photocell design is also spatially efficient, using in one embodiment only four MOSFETs in addition to the parasitic BJT. The embodiments of the invention are particularly useful in CMOS active pixel sensors used in imaging systems such as the digital camera.

Attorney's Docket No.: 042390.P4750

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Photodetecting Device Supporting Saturation Detection and Electronic Shutter

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

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Send correspondence to Eric S. Hyman, Reg. No. 30,139, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Eric S. Hyman, Reg. No. 30,139, (310) 207-3800.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Lawrence T. Clark**

Inventor's Signature _____ Date 2/26/98

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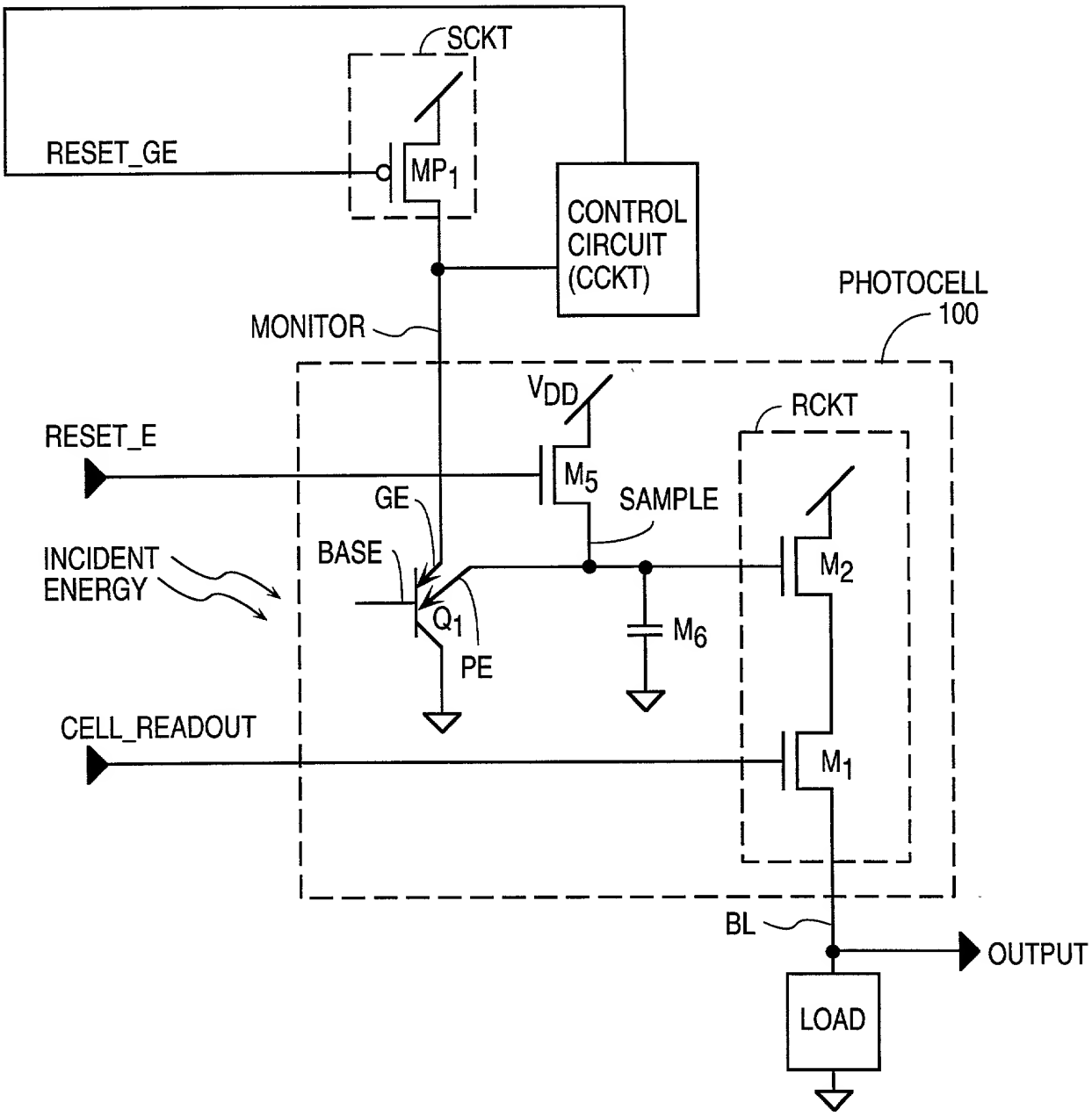

Fig. 1

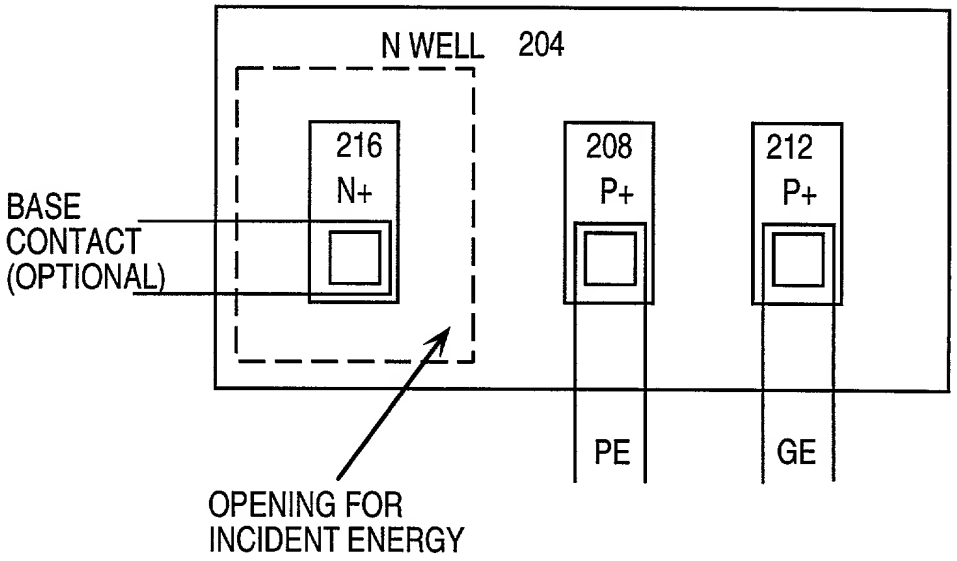

Fig. 2

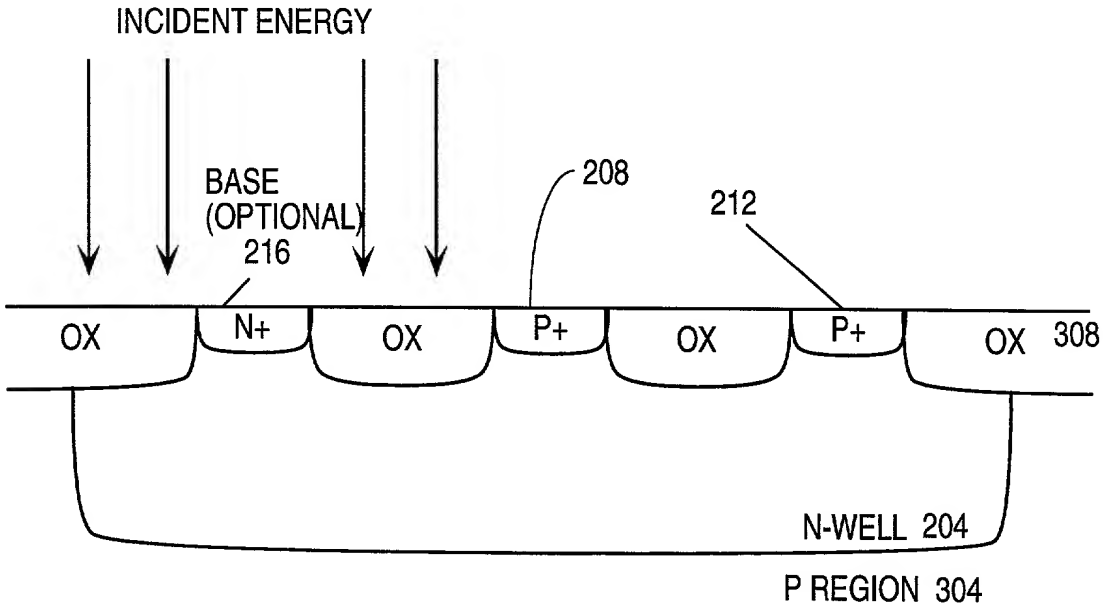

Fig. 3

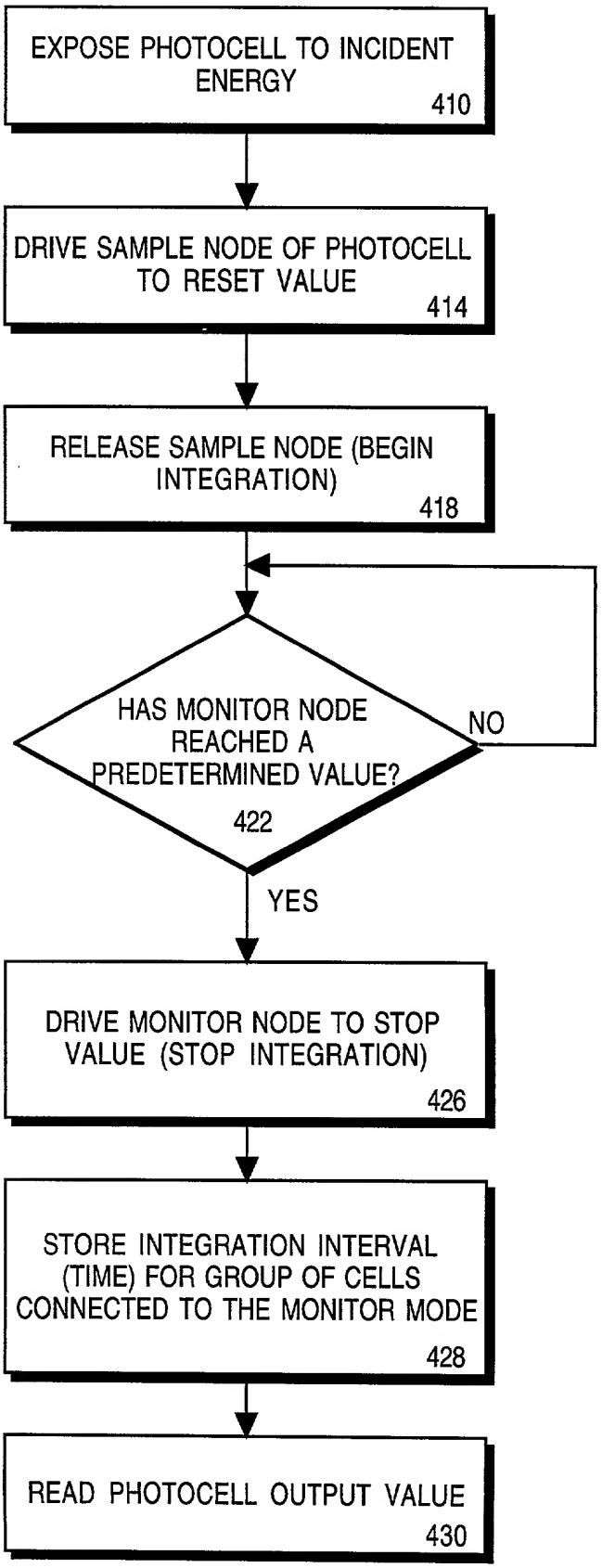

Fig. 4

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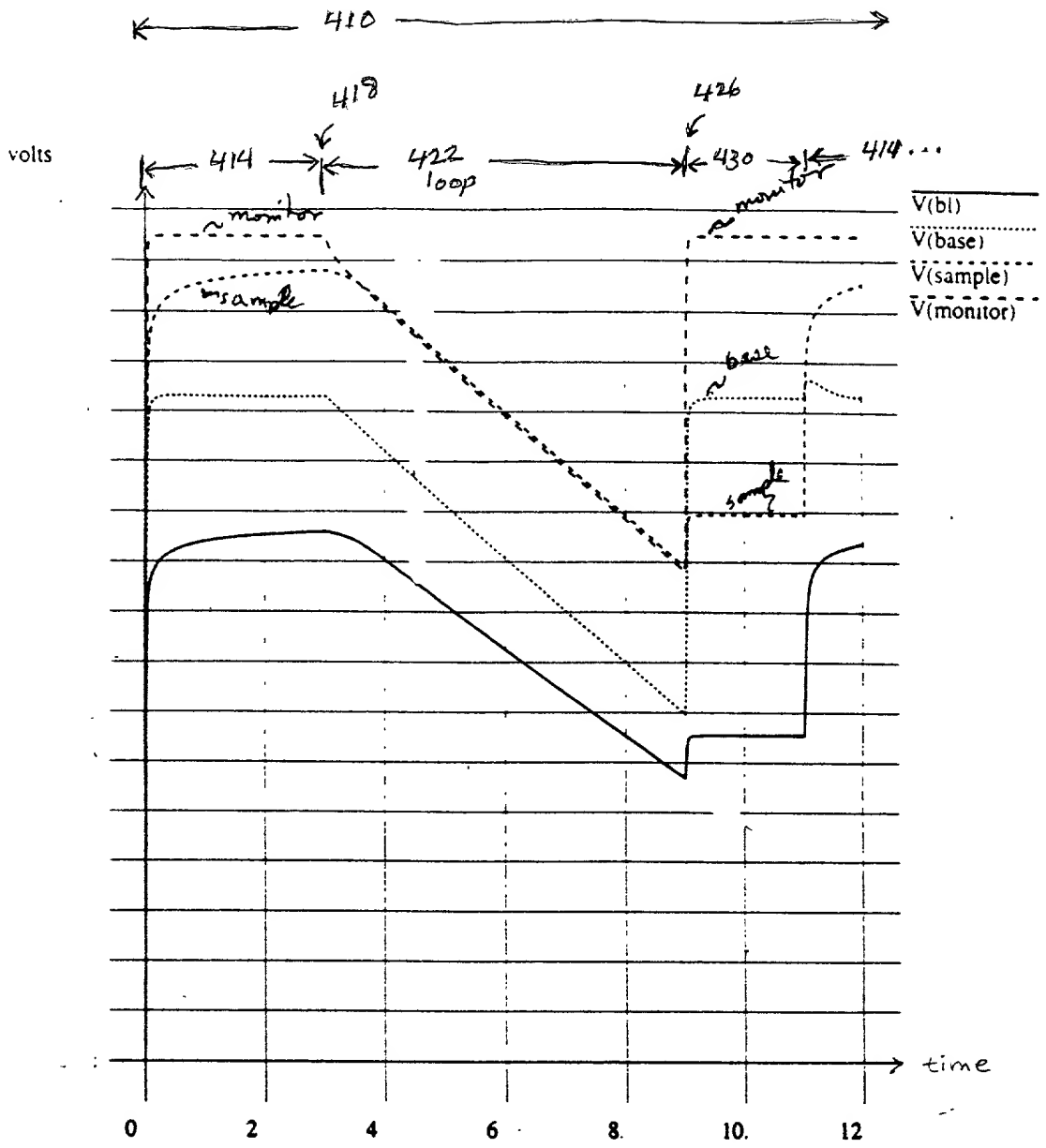
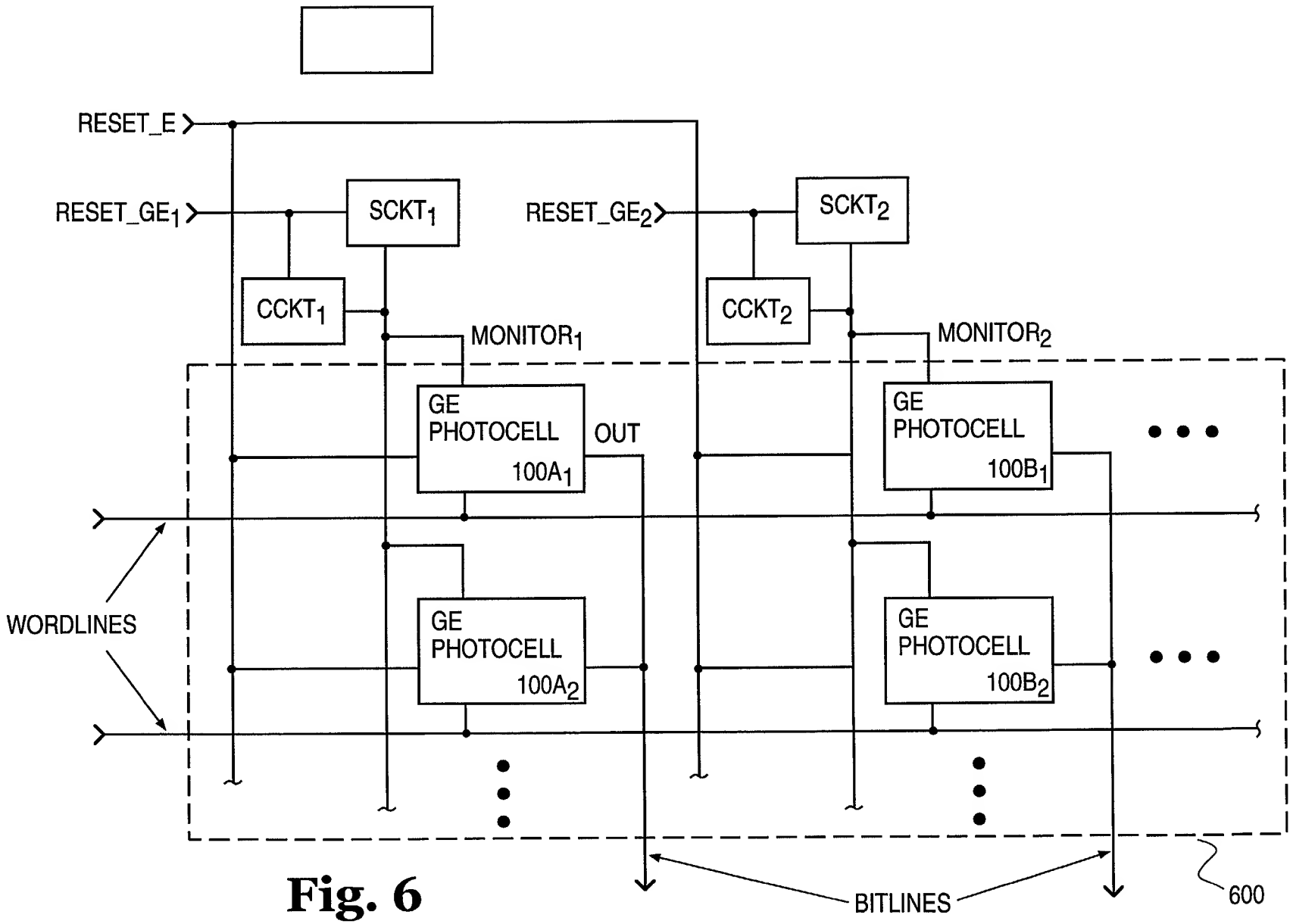


Fig-5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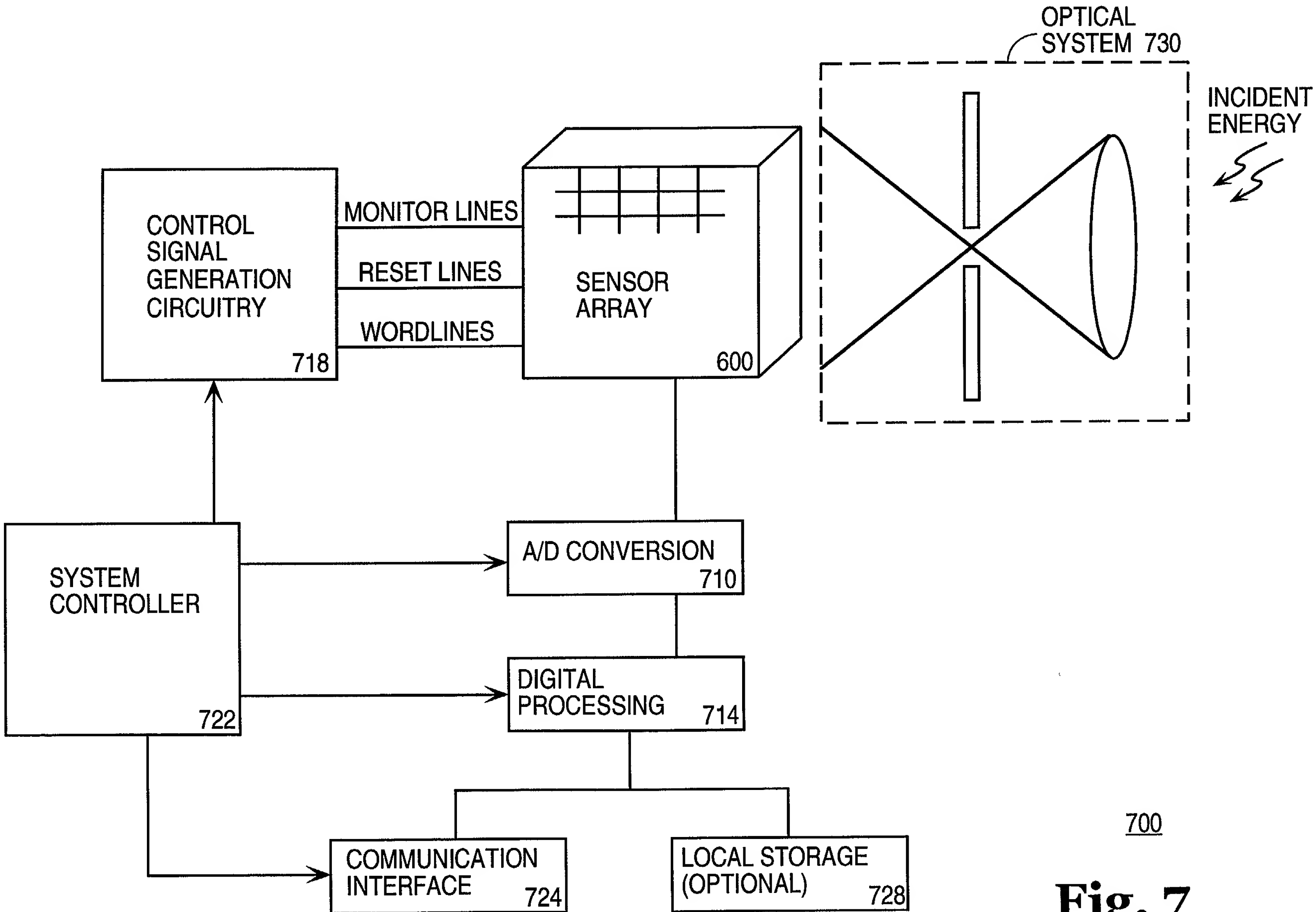
RESET_GE1
SCKT1
CCKT1
MONITOR1
RESET_GE2
SCKT2
CCKT2
MONITOR2
GE PHOTOCELL 100A1
OUT
GE PHOTOCELL 100B1
GE PHOTOCELL 100A2
GE PHOTOCELL 100B2
WORDLINES
BITLINES
600

Fig. 6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SIGNAL
GENERATION
CIRCUITRY
718
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RESET LINES
WORDLINES
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ARRAY
600
SYSTEM
CONTROLLER
722
A/D CONVERSION
710
DIGITAL
PROCESSING
714
COMMUNICATION
INTERFACE
724
LOCAL STORAGE
(OPTIONAL)
728
700

Fig. 7